REMARKS

Applicant appreciates the examination of the present application that is evidenced by the Official Action of August 14, 2002 (Paper No. 4). Nonetheless, Applicant admits some confusion with the Examiner's reliance on Japanese Published Application No. 06-45342 to Kanamori. Is the Examiner arguing that Kanamori discloses a base electrode in a trench or is the Examiner arguing that the floating field ring **21** within the trench **17** that is illustrated in the admitted prior art (AAPA) figure (FIG. 1) renders obvious the structure of a trench having a base electrode therein? Because Applicant is not sure how the Examiner is using Kanamori, Applicant will address both alternatives. For the convenience of the Examiner, Applicant has attached hereto an accurate translation of the Kanamori reference.

Applicant acknowledges that FIGS. 1 and 13 of the application both illustrate the use of floating field rings **21** within trenches **17** that are lined with insulating regions **19**. These floating field rings operate to electrically isolate a bipolar transistor from adjacent devices or regions within a semiconductor substrate and their use in providing isolation is well known to those skilled in the art. Applicant submits, however, that it is improper for the Examiner to identify an entirely extraneous structure, such as a trench-based floating field ring, in order to support an obviousness rejection of the claims. The trench-based floating field ring has absolutely nothing to do with a base region of a bipolar junction transistor and the Examiner has provided absolutely no support that there is any relationship between base regions and floating field rings.

Alternatively, if the Examiner is arguing that Kanamori discloses a base region or base electrode within a trench, then Applicant respectfully disagrees. As illustrated at paragraph [0009] of the attached Kanamori translation, the "graft" base region **5** is formed by thermally diffusing P-type dopants (boron) from the base polysilicon film **4a** into the substrate/collector **1**. Here, the term "graft" means "extrinsic". Applicant submits that this "graft" base region **5** in

Kanamori is essentially identical to the extrinsic base region **42** shown in prior art FIG. 2 of the application, because this extrinsic base region **42** is formed by diffusing P-type dopants from the P-type base electrode **23** into the intrinsic collector region **13**. (See, pages 3-4 of the application).

Thus, the Kanamori reference adds essentially nothing to the disclosure of the prior art illustrated by FIGS. 1-2 of the application. Accordingly, the Examiner has not established a prima facie case of anticipation or obviousness because none of the cited prior art references disclose or suggest the formation of a bipolar junction transistor having a trench-based base electrode or an extrinsic base region that is self-aligned to a base electrode that extends into an insulator-lined trench.

Applicant respectfully submits, therefore, that the present application is in condition for allowance. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**".

Respectfully submitted,

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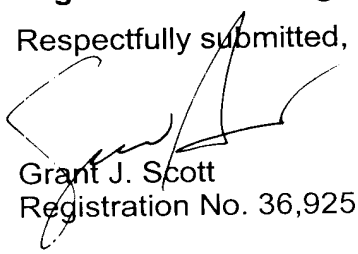
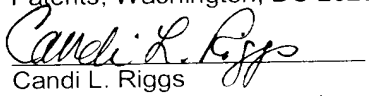


Grant J. Scott
Registration No. 36,925

Telephone: 919/854-1400
Facsimile: 919/854-1401
#278145

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX NON-FEE AMENDMENT, Commissioner for Patents, Washington, DC 20231, on November 11, 2002.



Candi L. Riggs
Date of Signature: November 11, 2002

Version with Markings to Show Changes Made

In the Claims:

The claims have been amended as follows:

28. (Amended) A bipolar junction transistor, comprising [the steps of]:

a semiconductor substrate having an intrinsic collector region of first conductivity type therein that extends to a surface thereof;

an electrically insulating layer on the surface of a semiconductor substrate, said electrically insulating layer having an opening therein and a lateral recess extending from the opening;

a trench that extends into the surface semiconductor substrate and the intrinsic collector region and is self-aligned to the opening in said electrically insulating layer;

a polysilicon base electrode of second conductivity type in the lateral recess and in the trench;

an extrinsic base region of second conductivity type that extends into the intrinsic collector and is self-aligned to a portion of the polysilicon base electrode that extends into the lateral recess; and

an emitter region of first conductivity type that extends in the intrinsic collector region.

* * * END * * *